REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on January 4, 2001, and the references cited therewith.

Claims 19-20, 53, 98, and 104-106 are amended, and claims 107-118 are added; as a result, claims 19-20, 53, 79-87, 98-102, and 104-118 are now pending in this application.

Election/Restriction

Applicant was requested to cancel claims 98-102 or to amend them in order to read on the elected embodiment of Figs. 1-7. Accordingly, Applicant has amended claim 98 to read on this elected embodiment.

§102 Rejection of the Claims

Claims 19, 53, 79, 80, 81, 87, 104, and 106 were rejected under 35 U.S.C. § 102(e) as being anticipated by Jeon (U.S. 6,025,257). This rejection is understood to be based on the premise that Jeon discloses a DRAM memory device having a capacitor structure comprising a first conductive plate, a dielectric layer formed on the first conductive plate, and a second conductive plate formed on the dielectric layer, wherein the dielectric layer is an oxide of the first conductive material. Applicant traverses the rejection.

Applicant makes no admission that the Jeon patent constitutes prior art, and reserves the right to swear behind Jeon. Nevertheless, Applicant believes the claims are patentably distinct from Jeon for the reasons set forth below.

Claim 19, as amended, recites a capacitor, comprising a first conductive plate, a second conductive plate, and a dielectric interposed between said first and second conductive plates, wherein said dielectric is an oxide of a metal layer overlying the first conductive plate. Jeon does not disclose the metal layer overlying the first conductive plate, and therefore does not disclose all of the limitations of claim 19. Accordingly, claim 19 is not anticipated by Jeon. Applicant respectfully requests that the rejection of claim 19 under 35 U.S.C. § 102(e) be withdrawn. Claims 79-81 depend from claim 19 and further define various embodiments of the present invention above the prior art; Applicant requests the removal of the rejection of claims 79-81 under 35 U.S.C. § 102(e) as well.

Similarly, claim 53 recites a capacitor that comprises a first capacitor electrode, a dielectric layer formed by oxidizing a metal layer overlying the first capacitor electrode, and a second capacitor electrode. Thus, claim 53 is also not anticipated by Jeon. Applicant requests that the rejection of claim 53 and of dependent claim 87 under 35 U.S.C. § 102(e) be removed as well.

The remarks above regarding claims 19 and 53 apply equally to claims 104 and 106. Applicant requests removal of the rejection of claims 104 and 106 under 35 U.S.C. § 102(e).

Claims 19, 53, and 81 were rejected under 35 U.S.C. § 102(b) as being anticipated by Cabral et al. (U.S. 6,625,233). The rejection is understood to be based on the premise that Cabral et al. discloses a capacitor structure comprising a first conductive plate, a dielectric layer formed on the first conductive plate, and a second conductive plate formed on the dielectric layer, wherein the dielectric layer is an oxide of the first conductive material. Applicant traverses the rejection.

Claim 19, as amended, recites a capacitor, comprising a first conductive plate, a second conductive plate, and a dielectric interposed between said first and second conductive plates, wherein said dielectric is an oxide of a metal layer overlying the first conductive plate. Cabral et al. does not disclose the metal layer overlying the first conductive plate, and therefore does not disclose all of the limitations of claim 19. Accordingly, claim 19 is not anticipated by Cabral et al. Applicant respectfully requests that the rejection of claim 19 and of dependent claim 81 under 35 U.S.C. § 102(b) be withdrawn.

Similarly, claim 53 recites a capacitor that comprises a first capacitor electrode, a dielectric layer formed by oxidizing a metal layer overlying the first capacitor electrode, and a second capacitor electrode. Thus, claim 53 is also not anticipated by Cabral et al. Applicant requests that the rejection of claim 53 under 35 U.S.C. § 102(b) be removed as well.

§103 Rejection of the Claims

Claims 20, 82-86, and 105 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Jeon (U.S. 6,025,257). This rejection is understood to be based on the premise that it would have been obvious to one of ordinary skill in the art to incorporate Jeon's DRAM memory device in the memory system as claimed. Applicant traverses the rejection.

As amended, claim 20 recites a memory system, comprising a monolithic memory device, comprising a capacitor, wherein the capacitor comprises a first conductive plate, a second conductive plate, and a dielectric interposed between said first and second conductive plates, wherein said dielectric is an oxide of a metal layer overlying the first conductive plate, and a processor configured to access the monolithic memory device.

As noted above in connection with claim 19, Jeon neither discloses nor suggests a metal layer overlying the first conductive plate. Accordingly, Jeon neither discloses nor suggests the invention as claimed in claim 20. Claim 20 is therefore patentably distinct from Jeon. Applicant requests that the rejection of claim 20 under 35 U.S.C. § 103(a) be removed. Claims 82-84 depend from claim 20 and are also patentably distinct from Jeon. Applicant requests the removal of the rejection of claims 82-84 under 35 U.S.C. § 103(a) as well.

Claims 85-86 depend from claim 53. Cabral et al. does not disclose the metal layer overlying the first conductive plate, and therefore does not disclose or suggest the present invention as recited in claim 53. Applicant requests the removal of the rejection of claims 85-86 under 35 U.S.C. § 103(a).

The above remarks relating to claim 20 apply equally to claim 105. Accordingly, Jeon neither discloses nor suggests the invention as claimed in claim 105. Claim 105 is therefore patentably distinct from Jeon. Applicant requests removal of the rejection of claim 105 under 35 U.S.C. § 103(a).

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6913 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 30 day of March, 2001.

Tina Pugh
Name

_____
Signature

Docket No. 303.455US3
WD # 353042

Micron Ref. No. 95-0505.02

CLEAN VERSION OF PENDING CLAIMS

DEVICES HAVING IMPROVED CAPACITANCE AND METHODS OF THEIR FABRICATION
Applicant: Karl M. Robinson
Serial No.: 09/470,265

Claims 19, 20, 53, 79-87, 98-102, and 104-118, as of March 30, 2001 (Date of Response to First Office Action).

Subt D'
C1

19. (Amended) A capacitor, comprising:

a first conductive plate;

a second conductive plate; and

a dielectric interposed between said first and second conductive plates, wherein said dielectric is an oxide of a metal layer overlying the first conductive plate.

20. (Amended) A memory system, comprising:

a monolithic memory device, comprising a capacitor, wherein the capacitor comprises:

a first conductive plate;

a second conductive plate; and

a dielectric interposed between said first and second conductive plates, wherein said dielectric is an oxide of a metal layer overlying the first conductive plate; and

a processor configured to access the monolithic memory device.

C2
C1

53. (Amended) A capacitor comprising:

a first capacitor electrode;

a dielectric layer formed by oxidizing a metal layer overlying the first capacitor electrode; and

a second capacitor electrode.

79. The capacitor of claim 19, wherein the first conductive plate is formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel.

80. The capacitor of claim 79, wherein the at least one metal is alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

81. The capacitor of claim 19, wherein the second conductive plate is formed from a material selected from the group consisting of polysilicon and metal.

82. The memory system of claim 20, wherein the first conductive plate is formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel.

83. The memory system of claim 82, wherein the at least one metal is alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

84. The memory system of claim 20, wherein the second conductive plate is formed from a material selected from the group consisting of polysilicon and metal.

85. The capacitor of claim 53, wherein the first capacitor electrode is formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel.

86. The capacitor of claim 85, wherein the at least one metal is alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

87. The capacitor of claim 53, wherein the second capacitor electrode is formed from a material selected from the group consisting of polysilicon and metal.

98. (Amended) A capacitor formed by a process comprising:

forming an insulative layer overlying a substrate;

masking the insulative layer to define a region in which to fabricate the capacitor;

removing the insulative layer in an unmasked region to expose a portion of the substrate;

depositing a polysilicon layer overlying the insulative layer and the substrate and contacting the substrate;

removing portions of the polysilicon layer to expose an upper surface of the insulative layer;

depositing a metal layer to overly the polysilicon layer, the metal layer being formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead;

contacting the metal layer with an electrolytic solution;

applying an electrical potential to the electrolytic solution and the metal layer;

oxidizing at least a portion of the metal layer to form a metal oxide to function as a dielectric layer; and

forming an electrically conductive layer overlying the metal oxide.

99. The capacitor of claim 98, wherein the electrolytic solution is a basic solution.

100. The capacitor of claim 98, wherein the electrolytic solution is an acidic solution.

101. The capacitor of claim 98, wherein the electrolytic solution is a solution of one part NH_4OH to ten parts water.

102. The capacitor of claim 98, wherein the electrolytic solution is a 0.1 molar solution of $HClO_4$.

Subt D5
C4

104. (Amended) A capacitor, comprising:

a first conductive plate formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel, alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead;

a second conductive plate formed from a material selected from the group consisting of polysilicon and metal; and

a dielectric interposed between the first and second conductive plates, wherein the dielectric is an oxide of a metal layer overlying the first conductive plate.

105. (Amended) A memory system, comprising:

a monolithic memory device comprising a capacitor, wherein the capacitor comprises

a first conductive plate formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel, alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead,

a second conductive plate formed from a material selected from the group consisting of polysilicon and metal, and

a dielectric interposed between the first and second conductive plates, wherein the dielectric is an oxide of a metal layer overlying the first conductive plate; and

a processor configured to access the monolithic memory device.

106. (Amended) A capacitor comprising:

a first capacitor electrode formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel, alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead;

a dielectric layer formed by oxidizing a metal layer overlying the first capacitor electrode; and

a second capacitor electrode formed from a material selected from the group consisting of polysilicon and metal.

107. (New) The capacitor of claim 19, wherein the metal layer comprises titanium.

108. (New) The capacitor of claim 19, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the metal layer.

109. (New) The memory system of claim 20, wherein the metal layer comprises titanium.

110. (New) The memory system of claim 20, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the metal layer.

111. (New) The capacitor of claim 53, wherein the metal layer comprises titanium.

112. (New) The capacitor of claim 53, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first capacitor electrode and the metal layer.

113. (New) The capacitor of claim 104, wherein the metal layer comprises titanium.

114. (New) The capacitor of claim 104, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the metal layer.

115. (New) The memory system of claim 105, wherein the metal layer comprises titanium.

116. (New) The memory system of claim 105, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the

metal layer.

117. (New) The capacitor of claim 106, wherein the metal layer comprises titanium.

118. (New) The capacitor of claim 106, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first capacitor electrode and the metal layer.